25. (New) The data processing device according to claim 14, wherein said instruction execution unit further includes a second register for holding said first control signal output from said instruction decoder and a third register for holding a second description indicating the condition,

said instruction execution unit performing the determination based on the second description held in said third register, reading the first control signal from said second register in response to the result of the determination, and executing the operation in accordance with the first control signal read from said second register.--

REMARKS

This Amendment responds to the Office Action dated October 24, 2000, in which the Examiner objected to the drawings and rejected claims 1-20 under 35 U.S.C. §102(a) or (e).

The drawings were objected to as not showing every feature of the invention claimed in the claims. Applicants respectfully traverse the Examiner's objection to the drawings and respectfully bring the Examiner's attention to Figures 9 and 11, which show the various timings for the invention. It is respectfully submitted that the drawings show every feature of the invention claimed in the claims. Therefore, it is respectfully requested that the Examiner withdraws the objection to the drawings.

As indicated above, the claims have been amended only to correct grammatical errors. It is respectfully submitted that the feature of the invention, that is delay of a time determining a condition, is not changed by the amendment to the claims.

Claims 1 and 14 claim a data processing device comprising an instruction decoder and an instruction execution unit. The instruction execution unit determines whether or not a predetermined condition is satisfied in a predetermined timing prior to executing the instruction. The prior art does not show, teach or suggest delaying of a time of determining a condition as claimed in claims 1 and 14.

Claims 1-20 were rejected under 35 U.S.C. §102(e) as being anticipated by *Holmann et al* (Japanese reference 410049370A) and rejected claims 1-20 under 35 U.S.C. §102(e) as being anticipated by *Holmann et al* (U.S. Patent No. 5,815,698).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102. The claims have been reviewed in light of the Office Action, and for reasons which are set forth below, it is respectfully requested that the Examiner withdraws the rejections to the claims and allows the claims to issue.

Holmann et al appears to disclose in Fig. 13 a basic format 320 of delayed branch instructions. Delayed branch instruction 320 comprises an opcode 321, a field 322 for designating a delayed value and a field 323 for indicating an offset or an address of a target branch address. (col. 13, lines 54-59) When the instruction decoder 8 in the instruction decode unit 8 recognizes that a decoded instruction is a delayed branch instruction, the instruction decoder unit 2 generates a control signal 11 and transfers it to the memory unit 3. In the memory unit 3, the PC controller 13 stores the decoded instruction into register 13A according to the control signal 11 received from the instruction decoder unit 2. Accordingly, the register 13A stores information indicating the target of a delayed branch instruction. The PC controller 13 stores a PC value related to the time when the branch

instruction will be executed into register 13B. When the value of the program counter (PC) in the microprocessor is equal to the value stored in register 13B, the PC controller 13 executes the branch instruction based on the target branch information stored in register 13A. That is, the value designated by the target branch information stored in register 13A is set into the program counter (PC). As a result, when the address of a fetched instructions is equal to the value stored in register 13B, the instruction at the target of a branch is fetched in the following cycles. (col. 14, lines 26-45, emphasis added)

Thus, *Holmann et al* merely discloses a microprocessor which can execute a delayed jump instruction where the field 322 designates the time for executing the branch instruction. Nothing in *Holmann et al* shows, teaches or suggests delaying the timing of the determination of a predetermined condition, as claimed in claims 1 and 14. Rather, *Holmann et al* merely discloses that the execution of the instruction is delayed. *Holmann et al* does not disclose delaying of the timing to determine the condition (i.e., an execution condition is not determined at a designated timing).

Since nothing in *Holmann et al* shows, teaches or suggests (a) decoding an instruction in a second period and determining the execution condition in a fourth period which starts after a certain duration of the second period as claimed in claim 1, or (b) a register storing a value representing a timing of starting to determine an execution condition and an instruction execution unit determining the execution condition in response to an event that the timing is detected based upon the value in the first register, as claimed in claim 14, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 14 under 35 U.S.C. §102(a) or (e).

Claims 2-13 and 15-20 depend from claims 1 and 14 and recite additional features. It is respectfully submitted that claims 2-13 and 15-21 would not have been anticipated by *Holmann et al* within the meaning of 35 U.S.C. §102(a) or (e) at least for the reasons as set forth above and since nothing in the reference shows, teaches or suggests determining an execution condition at the timing designated by a value in a third register as claimed in claim 6. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-13 and 15-20 under 35 U.S.C. §102(a) or (e).

New claims 21-25 have been added. It is respectfully submitted that these claims are also in condition for allowance.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the present invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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